In the Claims:

Please replace claims 18, 23, 35 -- 36 with the following:

18. A method, comprising:

powering up an integrated circuit:

loading a first data bit into a master latch during the powering up of the integrated circuit;

generating a second data bit from the first data bit:

latching the first data bit in the master latch; and

loading the second data bit into a slave latch.

23. The method of claim 18 wherein:

loading the first data bit into the master latch comprises generating a clock signal having a first clock state: and

latching the first data bit in the master latch and loading the second data bit into the slave latch comprise generating the clock signal having a second clock state.

35. A method, comprising:

powering up an integrated circuit:

loading a first data bit into a master latch during the powering up of the integrated circuit;

latching the first data bit in the master latch: and

loading the first data bit into a slave latch.

36. The method of claim 35 wherein:

loading the first data bit into the master latch comprises generating a clock signal having a first clock state: and

latching the first data bit in the master latch and loading the first data bit into the slave latch comprise generating the clock signal having a second clock state.

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